



# Electrical Transport and Optical Spectroscopy Discovery Platform

*CINT User Workshop Breakout Session, January 2007*

**Platform fabrication:** Malcolm Carroll, Kent Childs and David Luck

**External planning:** Mark Reed (Yale) and Dimitry Basov (UCSD)

**CINT scientists:** Michael Lilly, Aaron Gin, Elshan Akhador,  
Tom Picraux, Bill Smith, Rohit Prasenkumar, Alec Talin  
and Rick Averitt



# Outline

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- Discovery Platforms
- Electrical transport and optical spectroscopy concept
- First generation platform
- Discussion: features, additions and experiments



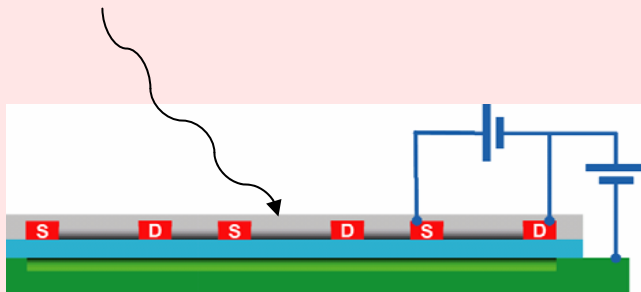
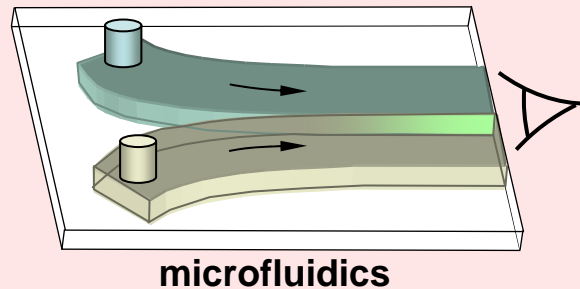
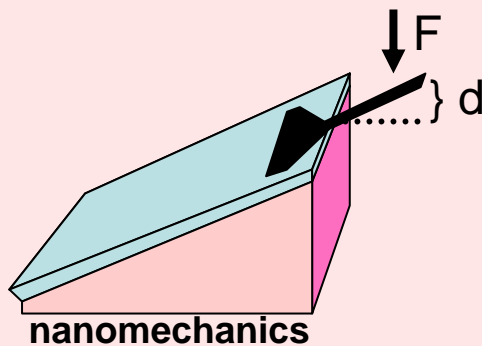
# Discovery Platforms: Unique User Capabilities For Nanomaterials Research

Discovery Platforms = “chips” that allow Users to:

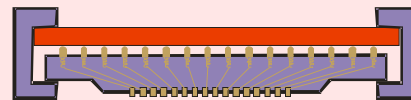
- Stimulate
- Interrogate
- Exploit

nanomaterials in microsystem environments

**CINT provides the platforms**



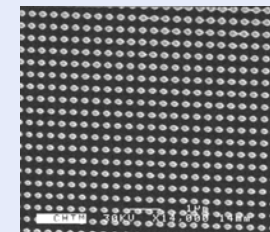
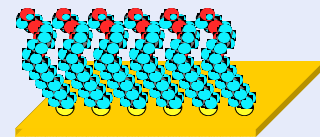
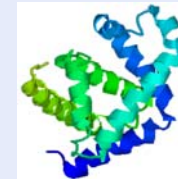
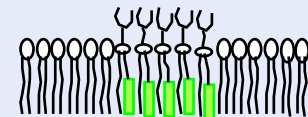
optical, transport



CINT instrument

packaging

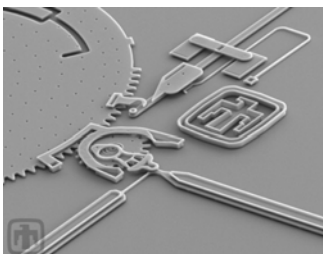
**Users provide the materials**



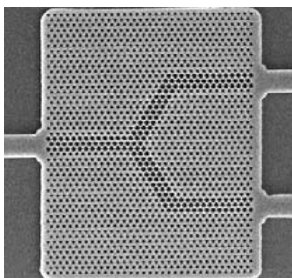


# Discovery Platforms

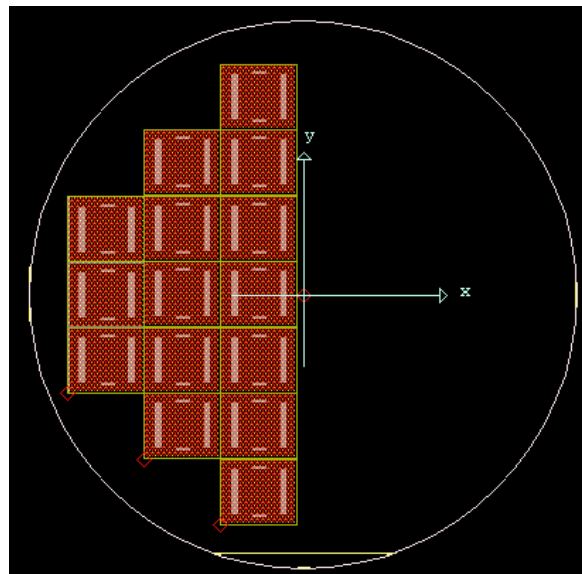
## Mechanics



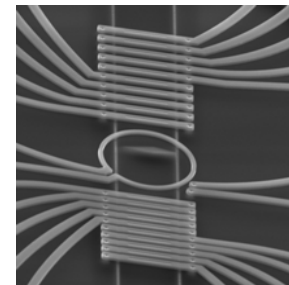
## Optics



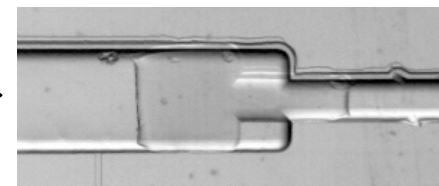
## Integrated Platform



## Electronics



## Fluidics



### Attributes:

- 1) Multiple in-out signals for stimulation, interrogation.
- 2) Standardized, readily available.
- 3) "Pop-In" Design for rapid utilization, exchange.
- 4) Rugged and robust.
- 5) Compatible with wide range of materials and CINT instruments.
- 6) Parallel architecture for statistics.
- 7) Controllable environment.

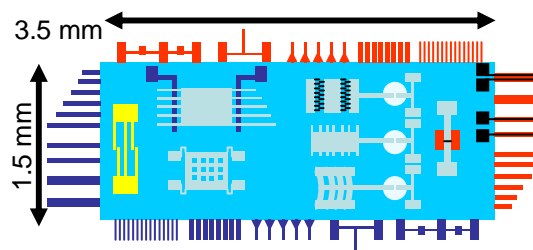


# New Tools: Discovery Platforms™

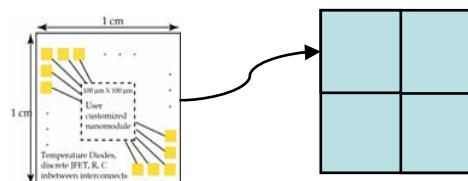
Standardized modular, micro-laboratories—designed and batch fabricated for:

- Integrating nano and micro length scales
- Studying the physical / chemical properties of nanoscale materials and devices
- Directly accessing wide range of CINT external diagnostic and characterization tools

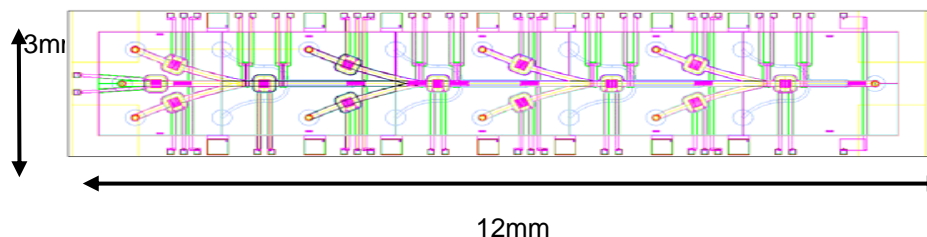
## Cantilever Array Platform



## Electrical Transport & Optical Spectroscopy Platform



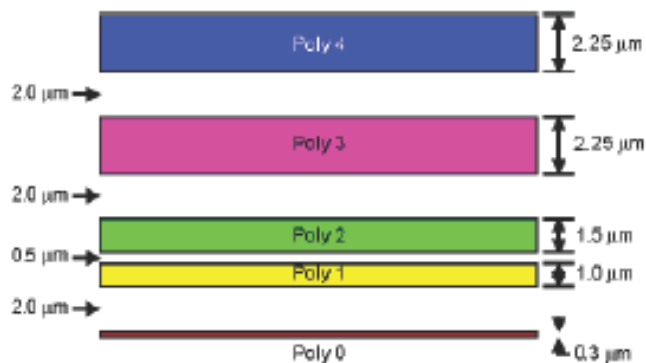
## Microfluidic Synthesis Platform





# Microsystems Development Lab

**SUMMiT V™** is a standard MEMS process at Sandia that enables rapid prototyping and production quantities of reproducible MEMS parts

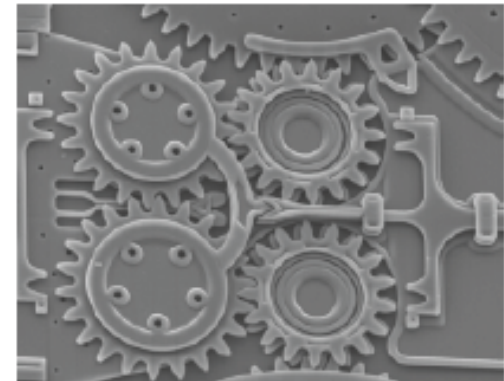


<http://www.sandia.gov/mstc/technologies/micromachines/tech-info/technologies/summit5.html>

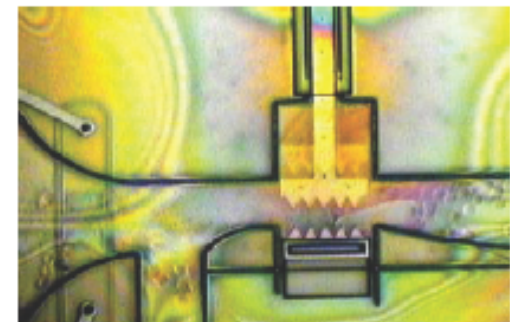
**SWIFT** is a MEMS process similar to SUMMiT, but it has the added feature of nitride encapsulation

- useful for microfluidics
- can also integrate simple transistors

*a complicated gear assembly made using SUMMiT V™*



*a microfluidic device made using SWIFT*





# Outline

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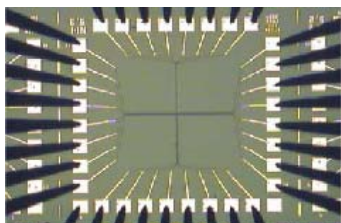
- Discovery Platforms
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# Initial Concept

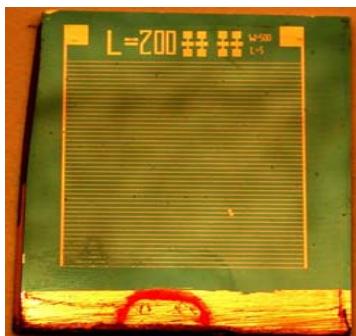
## *Microelectronics Platform for DC Transport*

*Courtesy of Mark Reed, Yale*



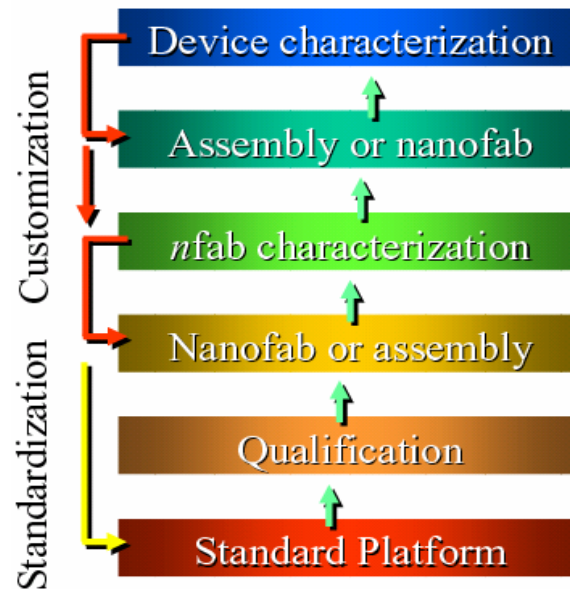
## *FET Structure for Electrostatic Doping*

*Courtesy of Dimitri Basov, USCD*



Goals:

- reliability
- throughput
- meaningful statistics





# Operational Characteristics

## **PLATFORM REQUIREMENTS:**

- *Wafer scale platform for multiple characterization runs → statistics*
- *Compatibility with automated screening to eliminate outliers*
- *Compatibility with 4-400K operation*

## **PLATFORM ATTRIBUTES:**

- *Supports DC transport, optical spectroscopy, and scanning probe measurements*
- *FET electrostatic doping to avoid disorder that occurs with chemical doping*
- *Future features could include on-chip amplifiers, or compatibility with electron microscopes*



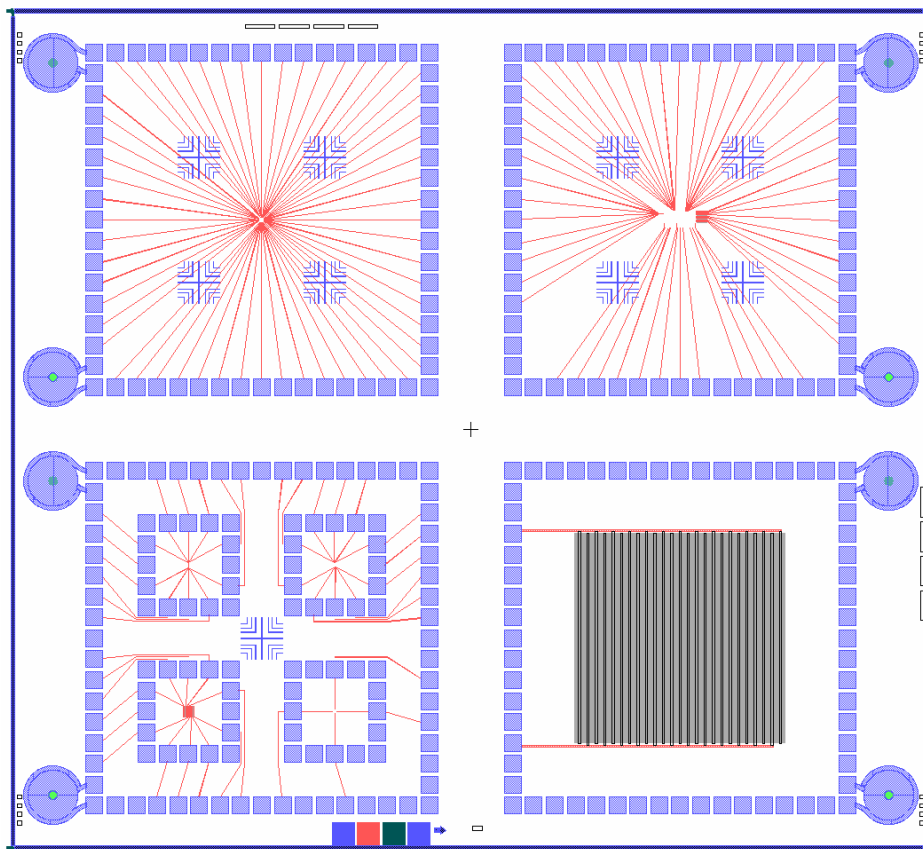
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# First generation overview



- Four quadrants
  - I – open for custom patterns (EBL)
  - II – lines and crosses
  - III – small die lines and crosses
  - IV – interdigitated fingers
- Features:
  - Back gate
  - Light sensor
  - Thermometer
- Key sizes:
  - Minimum feature size:  $0.18\ \mu\text{m}$
  - Overall – 2 cm x 2cm
  - 64 Contact pads,  $400\ \mu\text{m}$  square

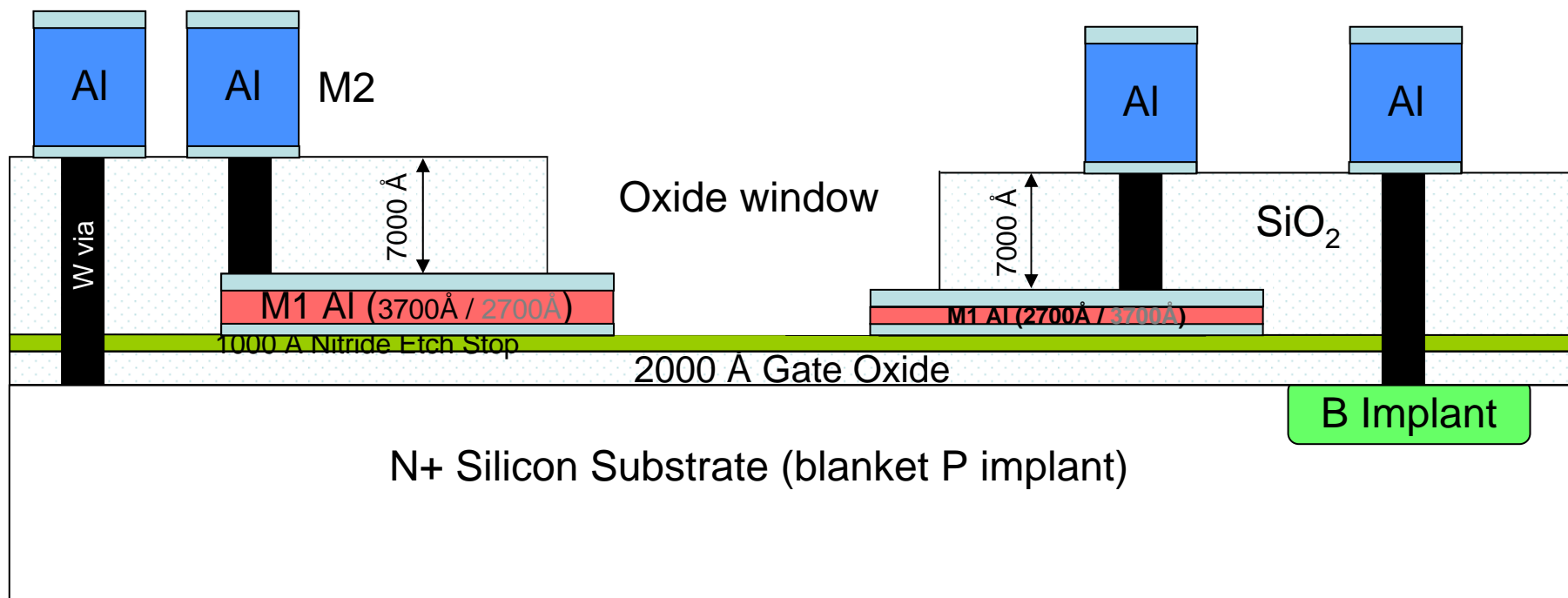


# Cross section

**M1** 200A Ti / 500A TiN / **2000A (or 1000A) Al** / 1000A TiN

**M2** 200A Ti / 500A TiN / **7000 A Al** / 1000A TiN

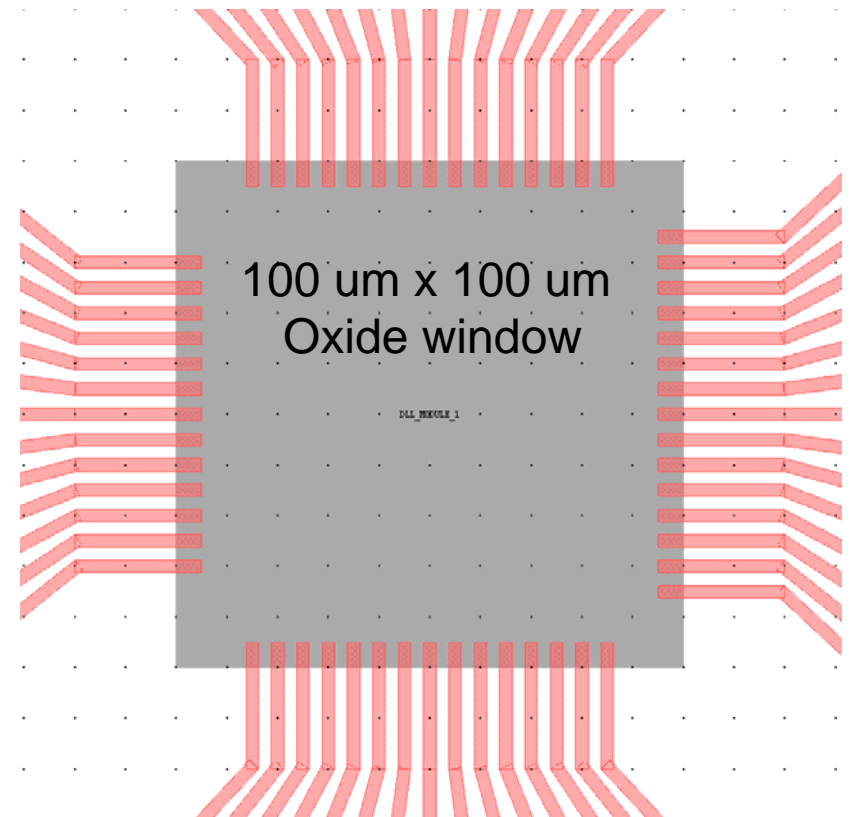
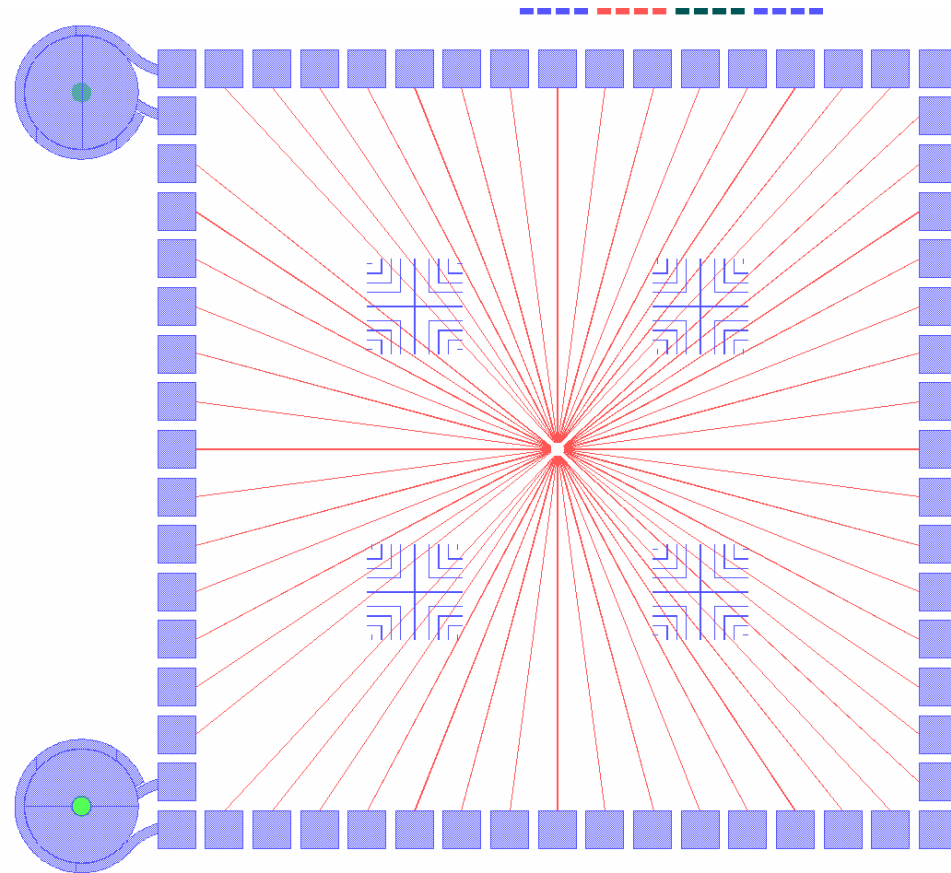
Gate oxide breakdown – 50 to 100 V (estimate)





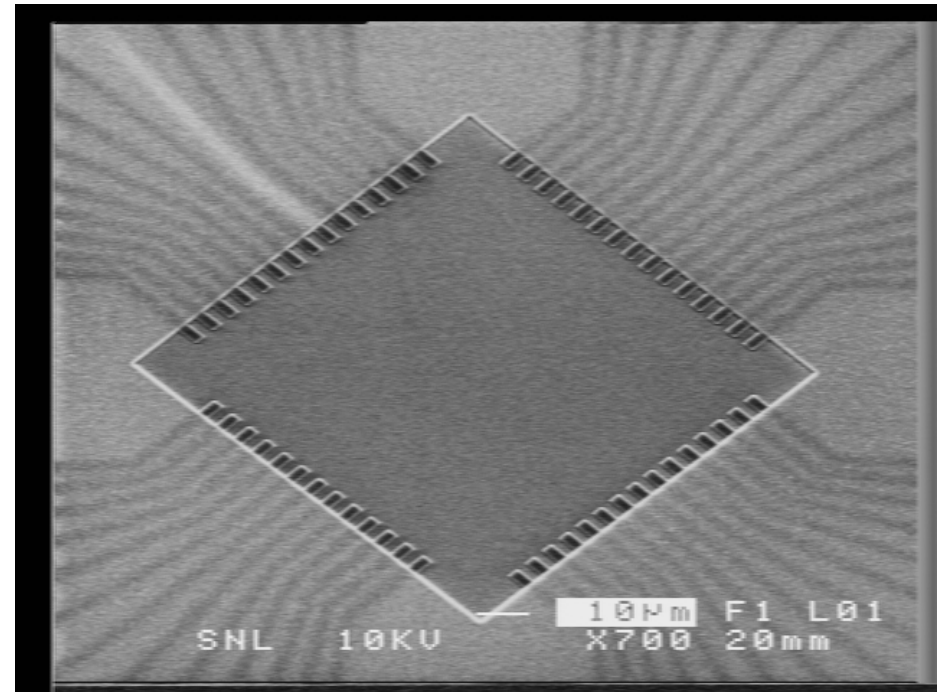
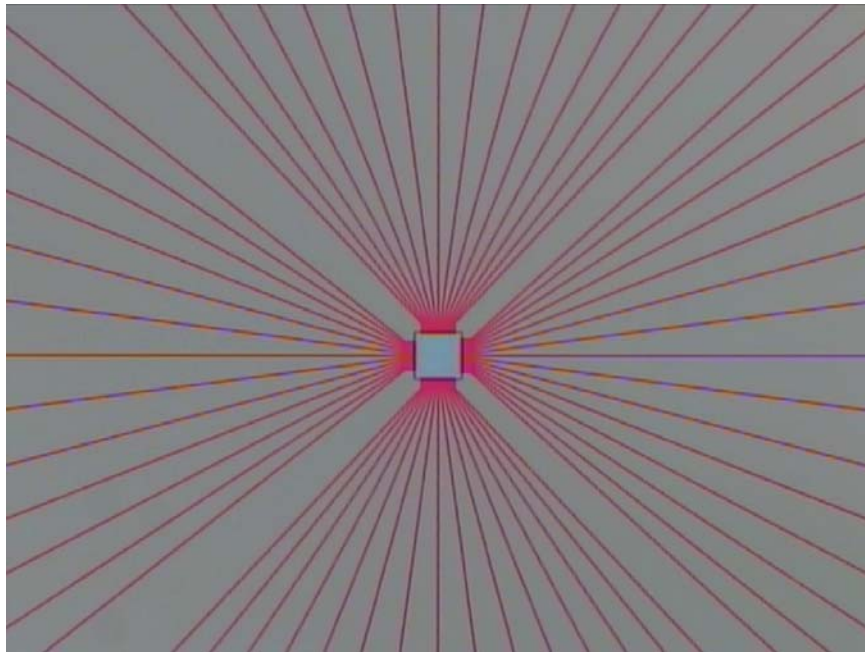
# Quadrant I: User Customizable

58 gate lines  
2.5um lines  
2.5um spacing



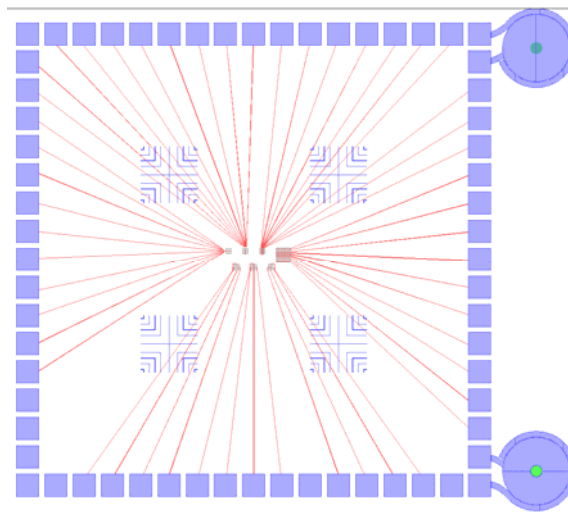


# Quadrant I images

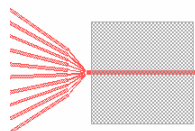




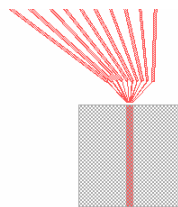
# Quadrant II: lines and crosses



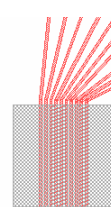
0.18um lines & spaces



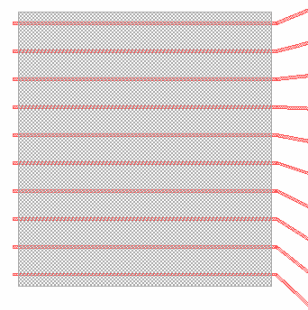
0.35um lines & spaces



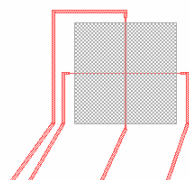
2.5um lines & spaces



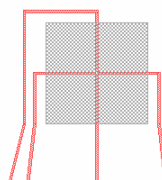
2.5um lines  
25um spaces



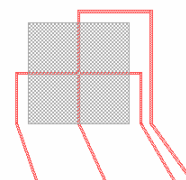
0.18um lines



0.5um lines

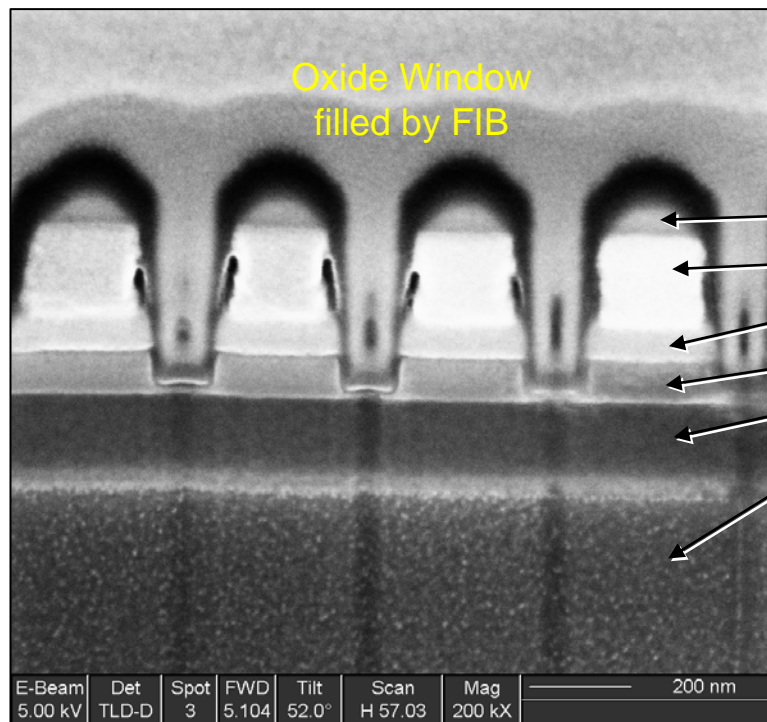
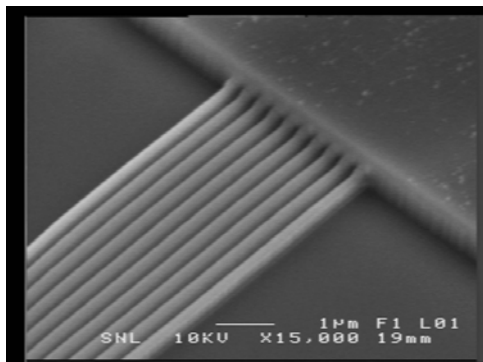
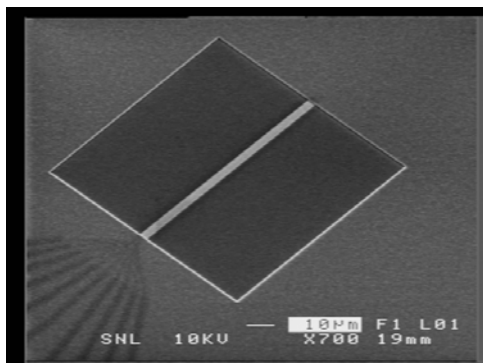


2.5um lines





# 0.18 $\mu\text{m}$ lines and spaces

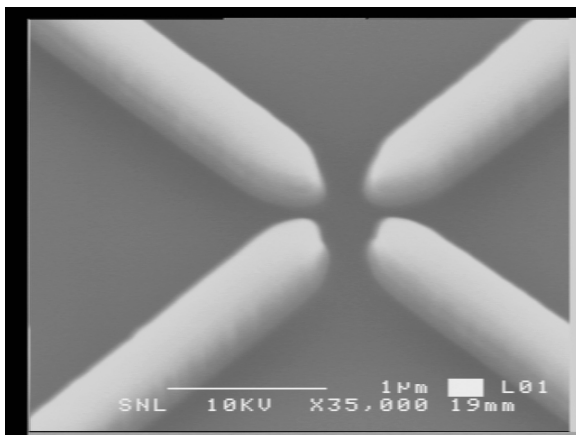




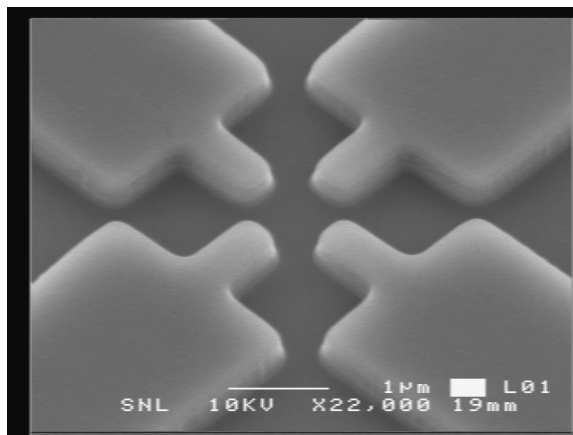
# Cross patterns

*4 gate crosses in quadrants II and III*

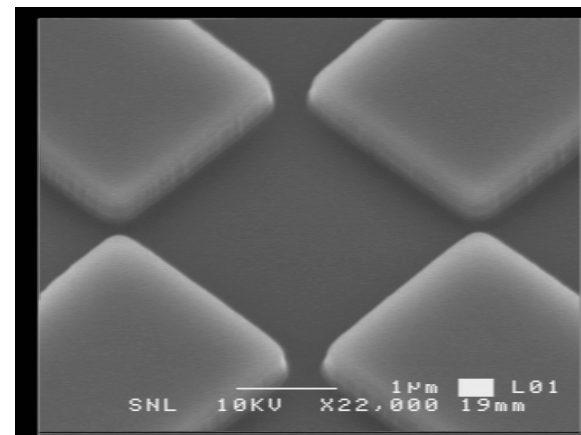
0.18  $\mu\text{m}$



0.5  $\mu\text{m}$



0.5  $\mu\text{m}$

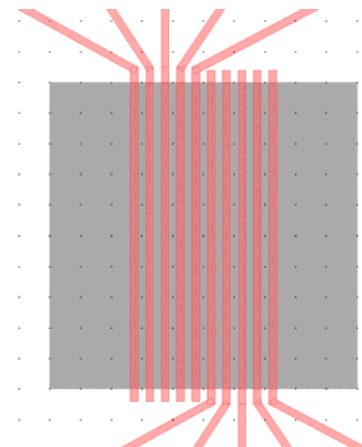
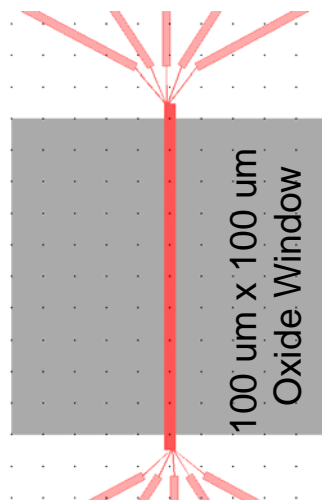
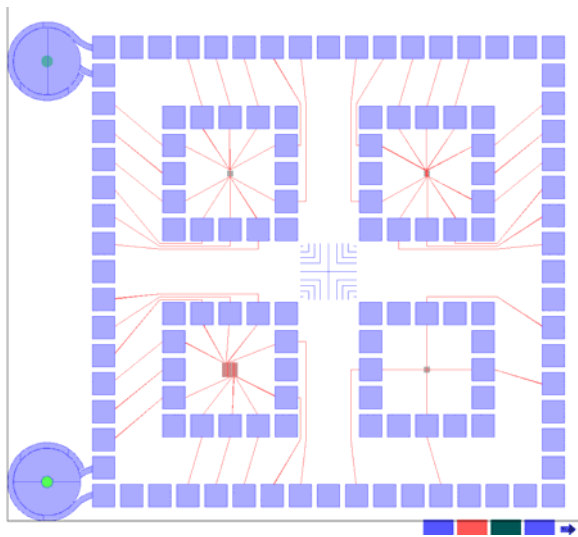




# Quadrant III: Small die

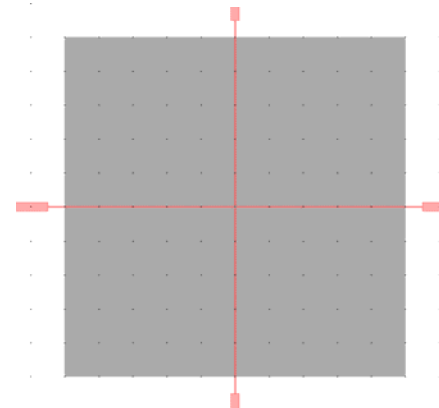
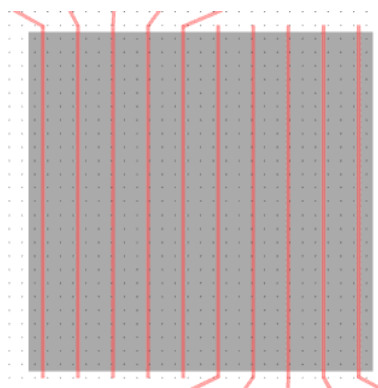
0.18  $\mu\text{m}$  lines & spaces

2.5  $\mu\text{m}$  lines & spaces



2.5  $\mu\text{m}$  lines & 25  $\mu\text{m}$  spaces

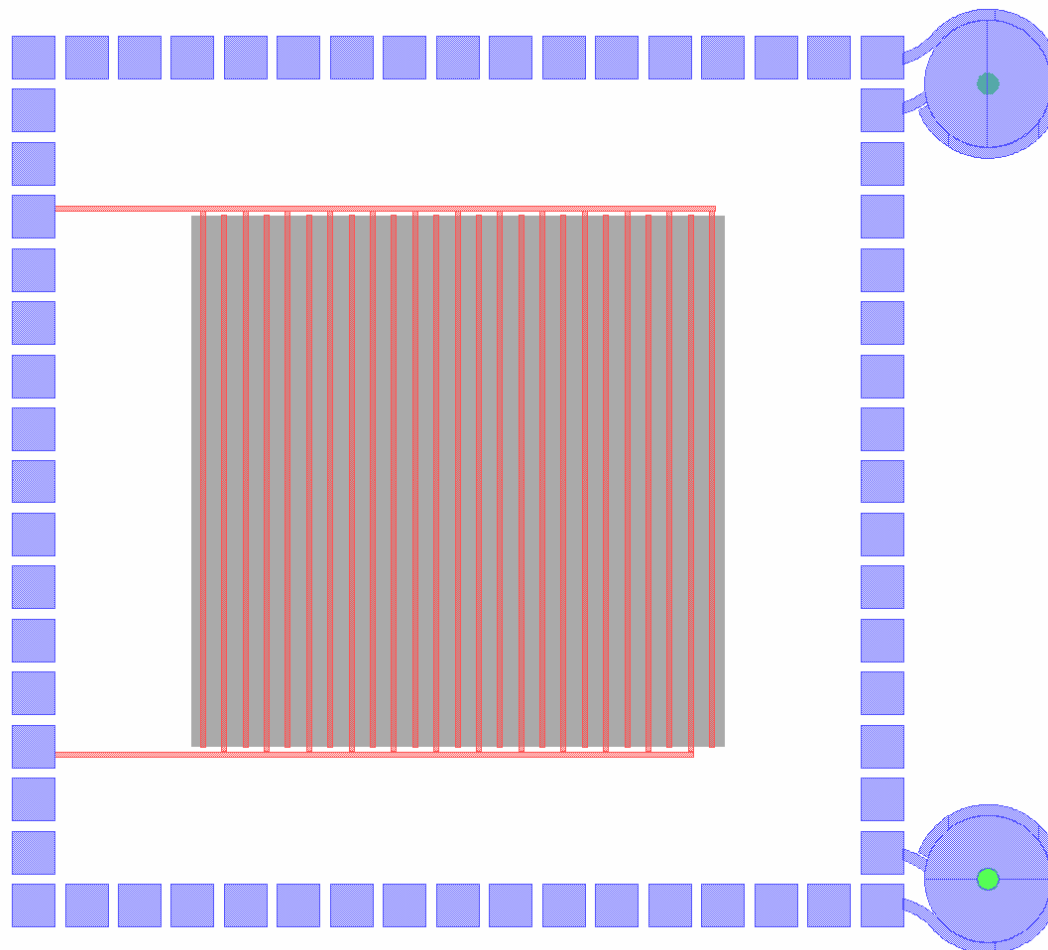
0.18  $\mu\text{m}$  terminated lines





# Quadrant IV: Interdigitated fingers

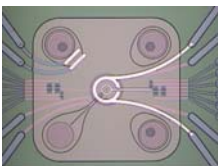
50  $\mu\text{m}$  interdigitated lines & 150  $\mu\text{m}$  spaces



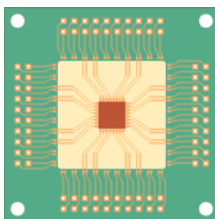


# Packaging and control electronics

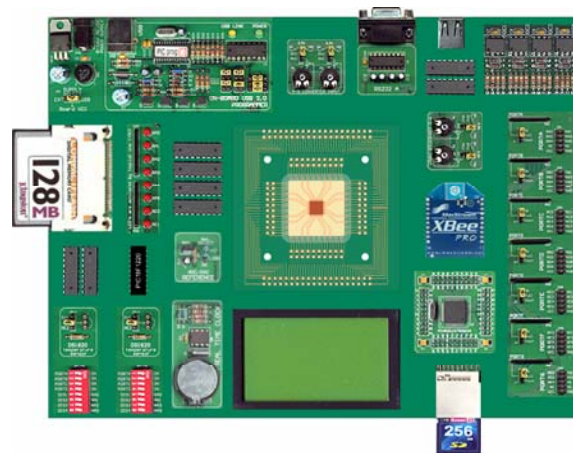
*platform*



*adapter*



*Instrument or integration base*





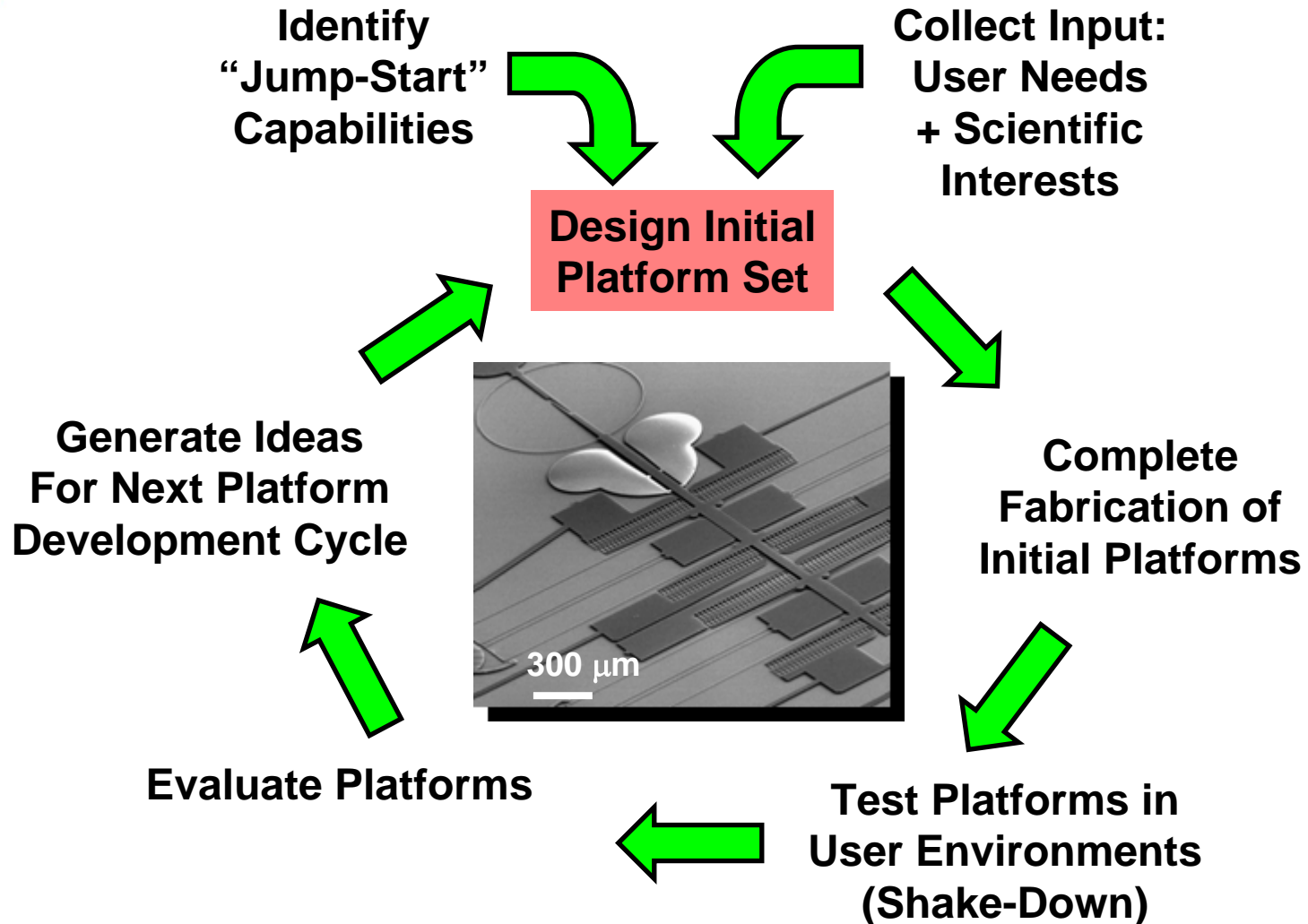
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# Discovery platform development cycle



Each step will require active collaborations and input from CINT scientists, platform developers, and the CINT User Community.

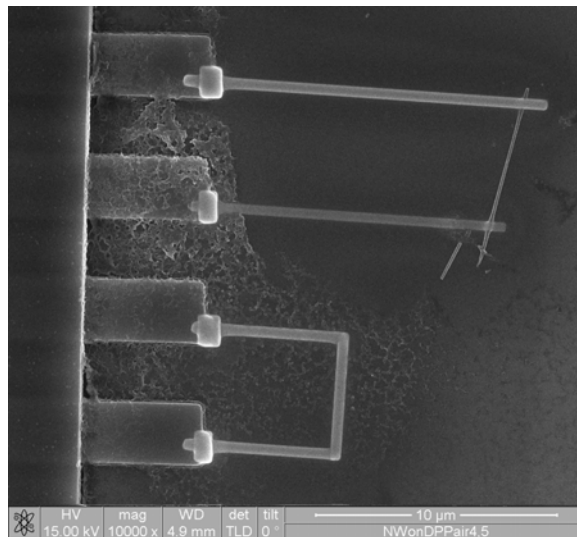


# Initial tests and experiments

Tests in progress:

- Diode characteristics for light and temperature sensing
- Line resistance, capacitance and leakage
- Contact properties
- Electron beam lithography region
- Surface characteristics (optics and AFM)

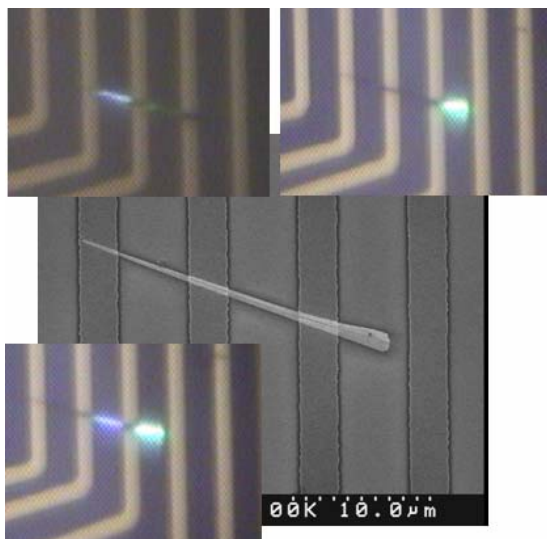
Example: *SiGe nanowire with FIB written Pt contacts*





# New capabilities – nanowire platform

*Alec Talin, CINT Integration Scientist*



- Nanowire dispersion
- Contact deposition (nanoimprint)
- Transport
- Micro photoluminescence



# Generation II

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- 2D electron channel (design work has already started)
- On-chip active components consistent with low temperature operation
- Implementation of nitride membranes
- ???